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First Named Inventor	Hsu
Art Unit	2134
Examiner Name	Tran, E.
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ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
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- ☐ Certified Copy of Priority Document(s)
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IN THE

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS:	Hsu et al.
APP. NO.:	09/896,255
FILED:	June 28, 2001
TITLE:	System And Method For Efficiently Performing A Data Encryption Operation
EXAMINER:	Tran, E.
ART UNIT:	2134
ATTY DKT NO:	50P4299.01/1575

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Dated: 10/5/06

Gregory J. Koerner

Reply Brief In Response To Examiner's Answer

Mail Stop Appeal Brief-Patents
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Dear Sir:

The following Reply to Examiner's Answer is submitted in response to an Examiner's Answer mailed August 9, 2006 in the above-referenced Application.

Remarks

On pages 1-8 of the Examiner's Answer mailed on August 9, 2006, the Examiner basically reiterates the same or similar language as was previously presented in the Final Rejection mailed on January 24, 2006, which is the subject of the Appeal Brief filed by the Applicants on June 7, 2006. However, on pages 8-16 of the Examiner's Answer, the Examiner presents a new section (10) entitled "Response to Arguments." Applicants herein provide responses to certain of the Examiner's remarks from the "Response to Arguments" section of the Examiner's Answer.

(A). Claims 1 and 21

On page 8 of the Answer, the Examiner maintains the previous rejections of independent claims 1 and 21. However, the Examiner concedes that Ober is limited to teaching "a standard direct memory address (DMA) controller . . . ." Applicants concur. Unlike Ober, Applicants however submit that their claimed "DMA engine" is not "standard" because it includes "an encryption module" that is internally implemented within the claimed DMA engine (see Applicants' FIG. 9).

In particular, claim 1 recites "*said DMA engine including an encryption module that . . .*" (emphasis added). Similarly, claim 21 recites "*processing source data with an encryption module of said DMA engine to . . .*" (emphasis added). Ober teaches that "[t]he cryptographic coprocessor is effectively broken

down into three major components: Input/Output (I/O) blocks 2, processor blocks 4 and security blocks 6" (column 4, lines 48-51). In addition to the foregoing "three major components", Ober teaches that "the co-processor may further include a standard direct memory access (DMA) controller circuit 42" (see column 4, lines 51-52). However, as explicitly shown in FIG. 1, the "security blocks 6" of Ober are *completely separate* from the DMA-32 controller circuit 42 of the cryptographic co-processor.

On page 8 of the Answer, the Examiner attempts to equate FIG. 6 of Ober to the "security blocks 6" shown within dashed lines in FIG. 1 of Ober. Applicants respectfully traverse. Applicants submit that the reference number "6" on FIG. 1 does not refer to FIG. 6 of Ober, but instead refers only to the "security blocks 6" described in column 4, lines 50-51 of Ober.

Furthermore, Applicants point out that Ober provides a discussion of FIG. 6 with the heading "DMA Controller Functional Description" (emphasis added) (see column 25, line 12). Based on the above-mentioned heading, Applicants submit that FIG. 6 portrays certain functions of the "DMA-32 controller 42" of FIG. 1 which does not include the "security blocks 6" as shown in FIG. 1. For at least the foregoing reasons, Applicants therefore submit that there is inadequate support for equating FIG. 6 of Ober to the "security blocks 6" in FIG. 1 of Ober.

On page 9 of the Answer, the Examiner states that the "subsystem" shown in FIG. 6 of Ober is "interpreted to be equivalent to the DMA engine of

the claimed invention." Applicants traverse. Using the identical language recited by Applicants in claims 1 and 21, Applicants submit that FIG. 6 of Ober explicitly discloses a "DMA engine" (shown in the bottom right quadrant of FIG. 6) with respect to which all other components in FIG. 6 are externally and not internally implemented. For at least the foregoing reasons, Applicants therefore submit that Ober *teaches away* from Applicants' invention.

In addition, Applicants submit that the "subsystem" shown in FIG. 6 of Ober includes elements that are clearly not part of a DMA engine. For example, in the upper left corner of FIG. 6, the disclosed "subsystem" includes digital signal processor (ADSP 2183). As illustrated and discussed in conjunction with FIG. 1 of Ober, the DSP core (ADSP 2183) is entirely separate and is not implemented within any type of DMA engine. Therefore, Applicants submit that it is inappropriate to equate the FIG. 6 "subsystem" to Applicants' claimed "DMA engine."

On page 10 of the Answer, the Examiner further states with regard to FIG. 6 of Ober, "notice this subsystem includes encryption and control registers." Applicants again traverse. Applicants submit that the "security blocks 6" shown in FIG. 1 of Ober are not shown anywhere in FIG. 6. On the contrary, Applicants submit that the "security blocks" of FIG. 1 communicate with the FIG. 6 subsystem through the 32-bit bus shown on the far-left of FIG. 6. The 32-bit bus shown in FIG. 6 is also shown in FIG. 1 of Ober as running horizontally, positioned below DMS-32 controller 42, and above blocks 32, 36,

30, 38, and 28 of the externally-implemented "security blocks 6." For at least the foregoing reasons, Applicants therefore respectfully submit that Ober fails to teach a "*DMA engine including an encryption module,*" as claimed by Applicants.

Because a rejection under 35 U.S.C. §102 requires that every claimed limitation be *identically* taught by a cited reference, and because the Examiner fails to cite Ober to identically teach the claimed invention, Applicants respectfully request reconsideration and allowance of claims 1 and 21.

(B). Claims 5-6 and 25-26

With regard to the rejections of claims 5-6 and 25-26, the Examiner cites column 11, lines 1-43 of Ober against various functionalities of Applicants' claimed "bridge device". Applicants again submit that Ober nowhere discloses a "bridge device" that performs the multiple specified functions that are recited in claims 5-6 and 25-26. In particular, Applicants submit that Ober nowhere discloses a bridge device that "facilitates bi-directional communications between said processor, one or more peripheral devices, said DMA engine, said encryption module, and said memory device" as recited in claims 5 and 25.

Furthermore, Applicants submit that Ober nowhere discloses a bridge device that "includes a processor interface for communicating with said processor, a memory interface for communicating with said memory device, and one or more peripheral interfaces for communicating with said one or more

peripheral devices," as recited in claims 6 and 26. For at least the foregoing reasons, Applicants request reconsideration of the rejections of claims 5-6 and 25-26.

(C). Claims 8 and 28

With regard to the rejections of claims 8 and 28, on page 3 of the Office Action, the Examiner cites column 31, line 52 through column 32, line 67, of Ober against various elements of Applicants' claimed "command structure". Applicants submit that, in contrast to Applicants' claimed command structure, the DMA registers discussed by Ober are provided only to control DMA data transfer operations, and have no effect upon *encryption* functionalities. For at least the foregoing reasons, Applicants therefore submit that Ober fails to disclose the "next command structure pointer" or a "control status command", as recited in claims 8 and 28. Applicants therefore respectfully request reconsideration of the rejections of claims 8 and 28.

(D). Claims 9 and 29

In the Appeal Brief, Applicants requested the Examiner to explicitly associate the claimed elements of claims 9 and 29 to specific teaching in Ober. Applicants note that, in the Examiner's Answer, there appears to be no responsive comments from the Examiner with regard to Applicants arguments for rejected claims 9 and 29. In the Final Office Action under Appeal, the

Examiner cited "tables 1 & 2, as well as claim 1" of Ober against various elements of Applicants' claimed "control status command". Applicants find no mention of the claimed elements of their "control status command" in either claim 1 or in tables 1 & 2 of Ober. Applicants therefore again respectfully request the Examiner to explicitly associate the claimed elements of claims 9 and 29 to specific teaching in Ober so that Applicants may respond appropriately, or alternatively, to withdraw the rejections of claims 9 and 29 under 35 U.S.C. 102.

(E). Claims 10 and 30

With regard to Applicants' arguments in the Appeal Brief regarding the "linked list" limitation of claims 10 and 30, the Examiner provides more than an entire page of somewhat vague remarks in the Answer, but fails to specifically address Applicants' arguments regarding in inappropriateness of associating a "linked list" to "parallel execution." The Examiner again cites column 5, line 41 through column 6, line 33 of Ober against Applicants' claimed "series of command structures that are linked together in a linked list to thereby perform a series of data encryption operations." On page 4 of the Final Office Action, the Examiner further states that Ober teaches encryption operations that are "performed at the same time or parallel execution which is interpreted to have the same meaning as 'linked list'."

In the "Free On-Line Dictionary Of Computing" (FOLDOC), a linked list is

defined as "[a] data structure in which each element contains a pointer to the next element, thus forming a linear list" (emphasis added). In the context of Applicants' encryption routines, Applicants submit that a linked list with a pointer to a "next" routine indicates that the encryption routines are intended to be executed in series, and not in parallel, as suggested by the Examiner. For at least the foregoing reason, Applicants submit that Ober fails to disclose encryption command structures that are linked together in a linked list, as recited in claims 10 and 30.

(F). Claims 11 and 31

Regarding the rejections of claims 11 and 31, as discussed above in conjunction with claims 1 and 21, Ober teaches only a "standard direct memory access (DMA) controller circuit" without any type of internal encryption functionality (see column 4, line 52). Ober therefore fails to disclose that "*said DMA engine includes a state machine for controlling said data encryption operation, one or more command registers for locally storing one or more command structures from said encryption structure, said control registers, a data buffer, an encryption key register, and said encryption module,*" as recited by Applicants in claims 11 and 31. In addition, Applicants submit that the command registers cited by the Examiner in Tables 1 and 2 of Ober are external and not internal to the DMA engine. Applicants therefore respectfully request reconsideration of the rejections of claims 11 and 31.

(G). Claims 12 and 32

In the rejections of claims 12 and 32, the Examiner cites "tables 1 & 2, as well as claim 1" of Ober against various elements of Applicants' claimed "control registers". In the Answer, the Examiner purports to explicitly associate the claimed elements of claims 12 and 32 to specific teaching in Ober. Applicants respectfully disagree with the Examiner's interpretation of the teachings of Ober.

On pages 14-15 of the Answer, the Examiner refers to various entries in Table 1 of Ober to support rejections of Applicants' claimed limitations with regard to their "start register," "halt/resume register," "clear interrupt register," link list register," and "status register." Applicants submit that none of the Table 1 entries cited by the Examiner provide control over a data encryption operation. In contrast, Applicants' claims 12 and 32 expressly recite that each of the foregoing registers are implemented to variously control or interface with "said data encryption operation."

In addition, the Examiner cites "Table 2 Status Registers" against Applicants' claimed "status registers." Applicants traverse. Applicants' independent claim 1, from which claim 12 indirectly depends, recites "said processor selectively programming control registers . . . ." In turn, claim 6 recites that "said control registers include . . . a status register . . . ." In contrast, Ober states that "[s]ome of the Registers are intended to be accessed only by the Secure Kernel and are referred to as Protected Registers (Table 2

below)" (emphasis added). Applicants therefore submit that the Status Registers of Table 2 are unable to be directly programmed by "said processor," as recited in claims 12 and 32. For at least the foregoing reasons, Applicants submit that the rejections of claims 12 and 32 under 35 U.S.C. 102 are improper.

(H). Claims 13 and 33

With regard to the rejections of claims 13 and 33, on page 2 of the Office Action, the Examiner cites column 7, lines 23-24 of Ober against Applicants' claimed "processor initially creating an encryption structure in said memory device." On page 15 of the Answer, the Examiner maintains the prior grounds of rejection. As support, the Examiner refers to a "Secure Download feature" mentioned in Ober. In particular, the Examiner states that "code may be downloaded into internal memory within the DSP . . ." (emphasis added).

Applicants submit that merely downloading code is not the same as actively "creating" an "encryption structure." Applicants also submit that the previously cited column 7, lines 23-24 of Ober is limited to discussing that the cryptographic co-processor "accesses the library and retrieves the particular encryption algorithm" (emphasis added). For at least the foregoing reasons, Applicants submit that Ober nowhere teaches a local processor device actively creating an encryption structure for use by a DMA engine, as recited in claims 13 and 33.

(I). Independent Claim 41

On page 16 of the Answer, the Examiner maintains the rejection of claim 41, and cursorily refers only to the claimed "means for creating an encryption structure." Applicants submit that claim 41 recites three other main elements in "means-plus-function" language that have not been addressed by the Examiner in the Answer. As previously discussed, "means-plus-function" language is utilized to recite elements and functionality similar to those recited in claims 1 and 21, as discussed elsewhere. Applicants therefore incorporate those remarks by reference with regard to claim 41. In addition, the Courts have frequently held that "means-plus-function" language, such as that of claim 41, should be construed in light of the Specification. More specifically, means-plus-function claim elements should be *construed to cover the corresponding structure, material or acts described in the specification*, and equivalents thereof.

In particular, independent claim 41 recites "means for creating an encryption structure in a memory device." The foregoing subject matter is discussed in the Specification, for example, at page 15, lines 1-3 (FIG. 9), and page 9, line 30 through page 12, line 3 (FIGS. 4-6). Claim 41 next recites "means for programming control registers to perform said data encryption operation." The foregoing subject matter is discussed in the Specification, for example, at page 15, lines 3-9 (FIG. 9), and page 13, line 17 through page 14, line 11 (FIG. 8).

Claim 41 further recites "means for accessing said encryption structure and said control registers to thereby control said data encryption operation." The foregoing subject matter is discussed in the Specification, for example, at page 15, lines 10-16 (FIG. 9). Claim 21 additionally recites "means for processing source data to produce destination data during said data encryption operation." The foregoing subject matter is discussed in the Specification, for example, at page 15, lines 17-25 (FIG. 9).

Applicants respectfully submit that, in light of the substantial differences between the teachings of Ober and Applicants' invention as disclosed in the Specification, claim 41 is therefore not anticipated or made obvious by the teachings of Ober. Because a rejection under 35 U.S.C. §102 requires that every claimed limitation be *identically* taught by a cited reference, and because the Examiner fails to cite Ober to identically teach the claimed invention, Applicants respectfully request reconsideration and allowance of claim 41.

(J). Claims 4 and 24

With regard to the rejections of claims 4 and 24, the Court of Appeals for the Federal Circuit has held that "obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion, or incentive supporting the combination." In re Geiger, 815 F.2d 686, 688, 2 U.S.P.Q.2d 1276, 1278 (Fed. Cir. 1987). Applicants submit that the cited references do not suggest a combination that

would result in Applicants' invention, and therefore the obviousness rejection under 35 U.S.C §103 is improper.

On page 16 of the Answer, in support of the rejections of claims 4 and 24, the Examiner cursorily states that "*Ober teaches a motivation to combine the references to utilize a small memory device to maintain security*" (emphasis added). Applicants respectfully submit that a *general restatement of the advantages disclosed by the Applicants* deriving from implementation of the present invention cannot act as the required teaching or suggestion to combine cited references for a proper rejection under 35 U.S.C. § 103. Courts have repeatedly held that "it is impermissible . . . simply to engage in *hindsight reconstruction* of the claimed invention, using the Applicants' structure as a template and selecting elements from references to fill in the gaps." In re Gorman, 18 USPQ 1885, 1888 (CAFC 1991).

For at least the foregoing reasons, the Applicants submit that claims 1-41 are not unpatentable over the cited references, and that the rejections are thus improper. The Applicants therefore respectfully request reconsideration and withdrawal of the rejections of claims 1-41.

SUMMARY

For all the foregoing reasons, it is earnestly and respectfully requested that the Board of Patent Appeals and Interferences reverse the rejections of claims 1-41, so that the present Application may be allowed and pass to issue in a timely manner.

Respectfully Submitted,

Hsu et al.

Date: 10/2/06 By: _____

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